

Quartus II Quick Start

To create a project:

- Menu → File → New Project Wizard
- Click "Next".
- Change the working directory to a blank folder or one that does not exist. (It will automatically be created.)
- Make up a name for your project. (Note: Remember your project name as you will need it later.)
- Click "Finished".
- Menu → Assignments → Settings
- Select "Simulator Settings"
- Change "Simulation mode" to "Functional".
- Click "OK".


If you want to create and test a schematic:

- Menu → File → New → "Block Diagram/Schematic File".
- Double click on blank grid to add objects
 - primitives\pins (input, output)
 - primitives\logic (and, or, etc)
- Design your schematic. (Hold control and drag to duplicate objects)
- Double click any object to change its name.
- Save the file (Note: The module name must be the same as your project name from above.)

If you want to create and test a Verilog file:

- Menu → File → New
- Select "Verilog HDL File".
- Click "OK".
- Type in or paste your Verilog code into the new window.
- Save the file (Note: The filename and module name must be the same as your project name from above.)
- Menu → Processing → Start Compilation (Ctrl + L)

To create a wave form file:

- Menu → Processing → Start → Start Analysis & Synthesis (Ctrl + K)
- Menu → File → New
- Select "Vector Waveform File".
- Double-click the left panel.
- Click "Node Finder..." button.
- Change the Filter to "Pins: all".
- Click "List" button.
- Click ">>" button to add all found pins to the list on the right.
- Click "OK".
- Click "OK".
- Menu → Edit → End Time.
- Change Time to an appropriate interval. (It is suggested to use the number of different data values times 10 ns so you have enough room to see the data.)
- Click "OK".
- Menu → View → Fit To Window.
- Use the "Wave Form Editing Tool"  to change input values by clicking and dragging over intervals.
 - Note: Outputs will have checked pattern so you can't change values.

To run the simulation:

- Menu → Processing → Generate Functional Simulation Netlist
- Menu → Processing → Start Simulation (Ctrl + I)
- The output waves should now be filled in. (Up is 1, down is 0)

Note: You can change the main file by right clicking on the filename and selecting "Set as Top-Level Entity." This can be a Schematic or Verilog file.